REMARKS

Claims 1-41 are currently pending. Claims 1, 6, 11, 19, 29, and 33 have been amended without acquiescence in the Office Action's basis for neither rejections nor prejudice to pursue in a related application. No new matter has been added. Support for the amendment can be found at least in paragraphs 25-26, 35-36 and 47-48.

Rejections Under 35 U.S.C. § 103

Claims 1-41 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Lee et al., U.S. Patent No. 6,430,731 (hereinafter "Lee") in view of Yalcin et al., U.S. Patent Publication No. 2003/0140324 (hereinafter "Yalcin"). Applicant respectfully traverses.

Independent claim 1, and similarly claims 6, 11, 19, 29 and 33, recites the following features:

> selecting, by using a processor, the first input timing event corresponding to the first output timing event as a worst case timing event if the first output timing event has a later arrival time of transitions at the output of the gate than the second output timing event and selecting the second input timing event corresponding to the second output timing event as the worst case timing event if the second output timing event has the later arrival time of the transitions at the output of the gate than the first output timing event such that one of a plurality of timing events propagated to the input of the gate with a worst output slew or output delay as a function of input slew at the output of the gate is selected as the worst case timing event (emphasis added).

Applicant respectfully submits that Lee in view of Yalcin fails to teach or suggest each and every feature of the present claims in a manner as recited therein. Specifically, Lee in view of Yalcin do not teach or suggest any input event that corresponds to the worst output event is selected as the worst case timing event.

Lee does not select any input signal as the worse case timing event by selecting the input signal that corresponds to the worst output signal. Lee merely calculates an envelope or boundary conditions and does not select any input event corresponding to its output event as the worst case timing event if the output event has the latest arrival time. Lee discloses in his background that the latest signal is selected to represent the worst case arrival time bound, and kept to carry through the circuit network. Lee does not consider that the latest signal at arrival may not be the worst case. Therefore, Lee does not teach or suggest at least "selecting, by using

a processor, the first input timing event corresponding to the first output timing event as a worst case timing event if the first output timing event has a later arrival time of transitions at the output of the gate than the second output timing event and selecting the second input timing event corresponding to the second output timing event as the worst case timing event if the second output timing event has the later arrival time of the transitions at the output of the gate than the first output timing event."

Yalcin is directed to functional timing analysis for characterization of virtual component blocks. Specifically, Yalcin provides for performing a timing analysis on virtual component blocks by using functional information obtained from the circuits control inputs and useful combinations. Yalcin performs timing analysis but does not select input signal as worse case timing event. Yalcin does not even hint at selecting the input signal with the worst case output signal as the worse case timing event at the input. Therefore, Yalcin also does not teach or suggest at least the feature of "selecting, by using a processor, the first input timing event corresponding to the first output timing event as a worst case timing event if the first output timing event has a later arrival time of transitions at the output of the gate than the second output timing event and selecting the second input timing event corresponding to the second output timing event as the worst case timing event if the second output timing event has the later arrival time of the transitions at the output of the gate than the first output timing event such that one of a plurality of timing events propagated to the input of the gate with a worst output slew or output delay as a function of input slew at the output of the gate is selected as the worst case timing event".

Therefore, Lee and Yalcin, singly or in combination, fail to teach or suggest the invention as a whole. Since the remaining claims depend from these independent claims 1, 6, 11, 19, 29 and 33, respectively, these remaining dependent claims are also allowable over the cited references for the same reasons discussed above with respect to claim 1.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

While rendered moot by the above reasons, the Applicant notes and formally states that to the extent there are any suggestions or statements of admissions of prior art or judicial notice of art by the Office Action, those implications of admission by Applicant or judicial notice by the Office Action are hereby traversed.

To the extent that any arguments and disclaimers were presented to distinguish prior art, or for other reasons substantially related to patentability, during the prosecution of any and all parent and related application(s)/patent(s), Applicant(s) hereby explicitly retracts and rescinds any and all such arguments and disclaimers, and respectfully requests that the Examiner re-visit the prior art that such arguments and disclaimers were made to avoid.

The Commissioner is authorized to charge any fees due in connection with the filing of this document to Vista IP Law Group's Deposit Account No. 50-1105, referencing billing number 02PA053US01. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Vista IP Law Group's Deposit Account No. 50-1105, referencing billing number 02PA053US01.

Respectfully submitted,

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